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COMPUTER-AIDED ELECTRONIC CIRCUIT DESIGN
PART II
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Status Report

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Electronic Systems Laboratory

MASSACHUSETTS INSTITUTE OF TECHNOLOGY, CAMBRIDGE 39, MASSACHUSETTS

Department of Electrical Engineering

December 1964 Status Report ESL-SR-225 Copy No. 15

(PART I)
COMPUTER-AIDED ELECTRONIC CIRCUIT DESIGN

and

(PART II)
CONDUCTION PROCESSES IN THIN FILMS

Status Report

June 1, 1964 - November 30, 1964

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PART I

COMPUTER-AIDED ELECTRONIC CIRCUIT DESIGN

CONTENTS

I. INTRODUCTION

Professor J. F. Reintjes

The research reported here was initiated at the Electronic Systems Laboratory, Massachusetts Institute of Technology, six months ago under a grant from the National Aeronautics and Space Administration, Office of Advanced Research and Development. Its objective is to exploit the digital computer as a tool for designers of electrical circuits, with emphasis on techniques that may ultimately benefit the space program.

The Electronic Systems Laboratory is currently undertaking an extensive research program in computer-aided design. Included in this work are problems related to mechanical design, the design of computer-language systems, and the development of oscilloscope displays and consoles to aid the designer in his communications with the computer. The research in computer-aided electronic-circuit design being reported upon here augments the total effort and extends the program into a realm heretofore not treated by the Laboratory.

The key feature of the approach being taken is that the designer himself retains a key role in the design process and uses the computer to augment and assist him in executing a design. Through the power of his design tool it is expected that the designer will gain a deeper insight into circuit performance than can be readily obtained through manual calculation. Circuit analysis and synthesis procedures carried out with the aid of a computer should yield designs whose ultimate performance and reliability are predictable with a high degree of confidence before the circuit is actually built and tested. With a computer available during the actual design interval, circuits can be evaluated over a wide range of simulated environmental conditions and with signals of widely varying dynamic range. Execution of designs can also be carried out rapidly with corresponding reduction in design cost.

In the conduct of the research, the group has had full access to M. I. T's Project MAC computer. Project MAC is a large-scale computer experiment on time-shared use of computers. Availability of a time-shared computer facility which readily permits man-machine interaction is a key item for economy and speed in the computer-aided design process. Currently an IBM 7094 computer has been modified for time-shared use. The basic units for man-computer communication are teletypewriters distributed remotely from the

machine and two oscilloscope display consoles with a light pen, a set of shaft encoders, and other mechanical actuators for supplying program-dependent inputs to the computer from the console.

To date the research on computer-aided circuit design has proceeded along the following lines. As a preliminary step to the initiation of specific tasks, contacts were made with groups inside and outside M. I. T. which might be engaged in efforts relating to our goals. Upon completion of this survey, work was started under the general headings of computer-aided circuit analysis, synthesis of logic circuits, and threshold logic. The status of each of these efforts is presented in this report.

II. COMPUTER-AIDED CIRCUIT ANALYSIS

A. SIMULATION OF NONLINEAR NETWORKS

Dr. Jacob Katzenelson
Staff Member

The object of this work is to obtain a digital-computer simulation program for nonlinear electrical networks. The computer program will have the ability to simulate a wide class of nonlinear circuits and will permit the user to act upon the circuit while it is being simulated, that is, he will be able to change parameters, observe results, and make further parameter changes after additional computation.

The user is assumed to have access to a time-shared computer through a typewriter and oscilloscope display unit. Through this equipment he is able to convey his instructions and have the results typed or displayed almost immediately. The program permits use of nonlinear resistors, capacitors, mutual and self inductors, and independent and dependent sources. These elements are specified by their characteristic curves. In the case of a resistor, the characteristic is a curve in the v, i plane, whereas in the case of a current-controlled current source it is a curve in the i_1, i_2 plane. A device such as a transistor is presented to the computer through specification of its equivalent circuit in terms of the above components.

In his communications with the machine, the user employs terminology of circuit theory. He addresses the machine in terms of component names, specifies their connections to form a network, and connects subnetworks to form a larger network. As output information, he may ask for the voltage at any node or for the current through any branch. After the computation is finished, the computer displays the required result on an oscilloscope display unit. It is possible for the user to omit or change existing components, add different elements to the network, and have the computer calculate the network again with the new data.

The user supplies information to the computer either by drawing on the oscilloscope by means of a light pen or by typing in a list of active and passive components and their connections. From this list, the network equations (ordinary differential equations) are automatically set. The next step is numerical integration of the equations and subsequent display of the results.

If the user requires a change in the network, for example, the introduction of additional components, the program after being informed, changes the network equations and proceeds in solving the new system.

It is of interest to make a comparison between the proposed system with simulation through use of an analog computer. Once computer time-sharing, oscilloscope display, and a special "circuit language" are used, digital-computer simulation is as simple and direct as analog simulation. However, the digital computer has the advantage of a larger dynamic range and it is more flexible and able to store nonlinear functions in a simple manner.

The theoretical studies for this research were completed by the investigator before joining the Electronic Systems Laboratory staff. They include studies of the existence of solution of networks constructed from nonlinear components[1] and a study of the time required for solving a large network of nonlinear resistors. The plan for future work at the Electronic Systems Laboratory is as follows: Initially, concentration will be on the development of the computer program which establishes network equations for nonlinear RLC networks and solves them. Later, work will include programming the oscilloscope display system to display the network diagram and the calculated voltages and currents, theoretical work on nonlinear network theory, and application of the system to actual problems in design of electronic circuits.

B. AN ITERATIVE APPROACH FOR NETWORK ANALYSIS

Professor M. L. Dertouzos
Mr. Charles Therrien -
Fellowship Student

This work involves a study of a specific method for computer analysis of nonlinear passive networks, under dynamic conditions. The method makes possible the determination of any desired current or voltage waveform in a network excited by arbitrary voltage and current sources, and it bears some

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[1] Desor, C. A. and Katzenelson, J., "Nonlinear RLC Networks," Bell System Technical Journal, January, 1965.

resemblance to other iterative and relaxation techniques for network analysis.[2,3]

The over-all dynamic problem is reduced to n static problems by sampling at n discrete time intervals and by expressing the dynamic behavior of each component by a state and by means for updating that state. For example, a capacitor becomes equivalent to a voltage source (the state) and a series resistor (the updating mechanism), an inductor to a current source and a parallel resistor, and an arbitrary nonlinear energy storage element to a memory function and to a memory-dependent piecewise-linear expression for updating that function.

The static problem is then "solved", that is, voltages and currents are established throughout the network by the following iterative process. At any time interval, all nodes are assigned the voltages obtained by the solution of the network at the preceding time interval. If this is the first time interval, then all node voltages, except for those governed by independent sources, are assigned zero volts. Branch currents are then computed on the basis of the assigned voltages, and the algebraic sum of these currents, called the residue, is obtained at each node. (In general, this residue will be nonzero, unless the initial node-voltage assignment happened to be a valid solution.) At each node, the node voltages are then perturbed by adding the magnitude of the above residue, scaled by a constant K, in a direction that tends to decrease the magnitude of the new residue. The above process is then iterated until the successively perturbed node potentials satisfy an error convergence criterion (for example, the sum of the residue magnitudes over all nodes becomes less than a given tolerable bound), and the method terminates for that time interval.

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[2] Fadeeva, V. M., Computational Methods of Linear Algebra, Dover Publications (1959), pp. 17, 30.

[3] Birkhoff, G. and Diaz, J. B., "Nonlinear Network Problems," Quarterly of Applied Mathematics, Vol. 13, (Jan. 1956), pp. 431-443.

Thus far, we have shown that for any linear network, and for any nonlinear network where the v, i, nonlinearities are monotonically increasing, there exists a range of positive constants K, such that the above method converges onto a valid solution. Since it is eventually desired to examine the amount of computer time and space needed for executing the above method, several examples have been explored, using the Project MAC digital computer. One such example is the simple network shown in Fig. 1. In this example, the computer program started with the convergence constant K = 1.0 and decreased K successively by 0.1 until the current error (sum over all nodes of the squared residue) decreased between successive iterations (K = 0.1). The resulting value of the node voltages E_1, E_2, E_3, and of the current error are plotted in Fig. 1 as a function of the number of iterations. Figure 2 shows the current error as a function of the number of iterations with K as a parameter. The average slope magnitude, m, of each line in this figure, represents the reciprocal convergence time constant for that value of K. Observe that optimum convergence occurs in the vicinity of K = 0.2. Computer time necessary for a bad initial guess (50 volts) when the real solution was of the order of 2 volts was comparable to the time needed for exact solution by matrix inversion. Starting closer (0 volts) to the exact solution achieved convergence in half the time required for exact solution. Any conjectures as to relative convergence time between the given method and an exact method (in the case of linear networks) would be premature at this time. However, the preliminary results on convergence time, as well as the apparent simplicity with which the simulation can be altered as the network is altered, suggest the need for further study of the above method.

In the future it is planned to explore the capabilities and limitations of the cited method progressively in terms of networks having the following components: linear and nonlinear resistors, linear and nonlinear energy-storage elements, and linear and nonlinear active elements. It is also expected that the work will be implemented with input-output means as outlined in the previous section and will comprise evaluation of refinements on the values used for K in order to improve convergence, expended computer effort relative to other methods, and internal computer structure suitable for storing and processing the required information.

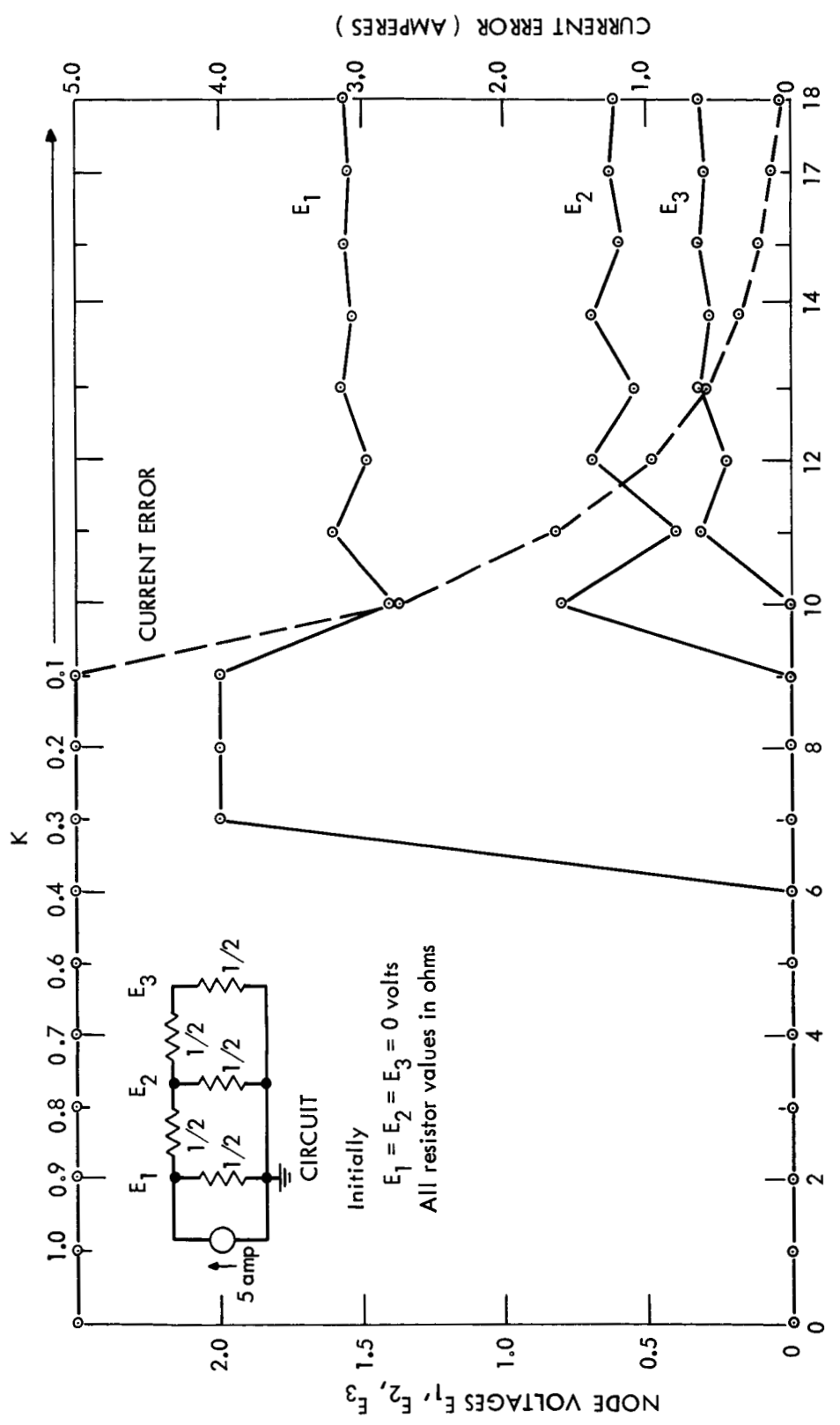


Fig. 1 CURRENT ERROR AND NODE VOLTAGES vs ITERATION NUMBER AND K

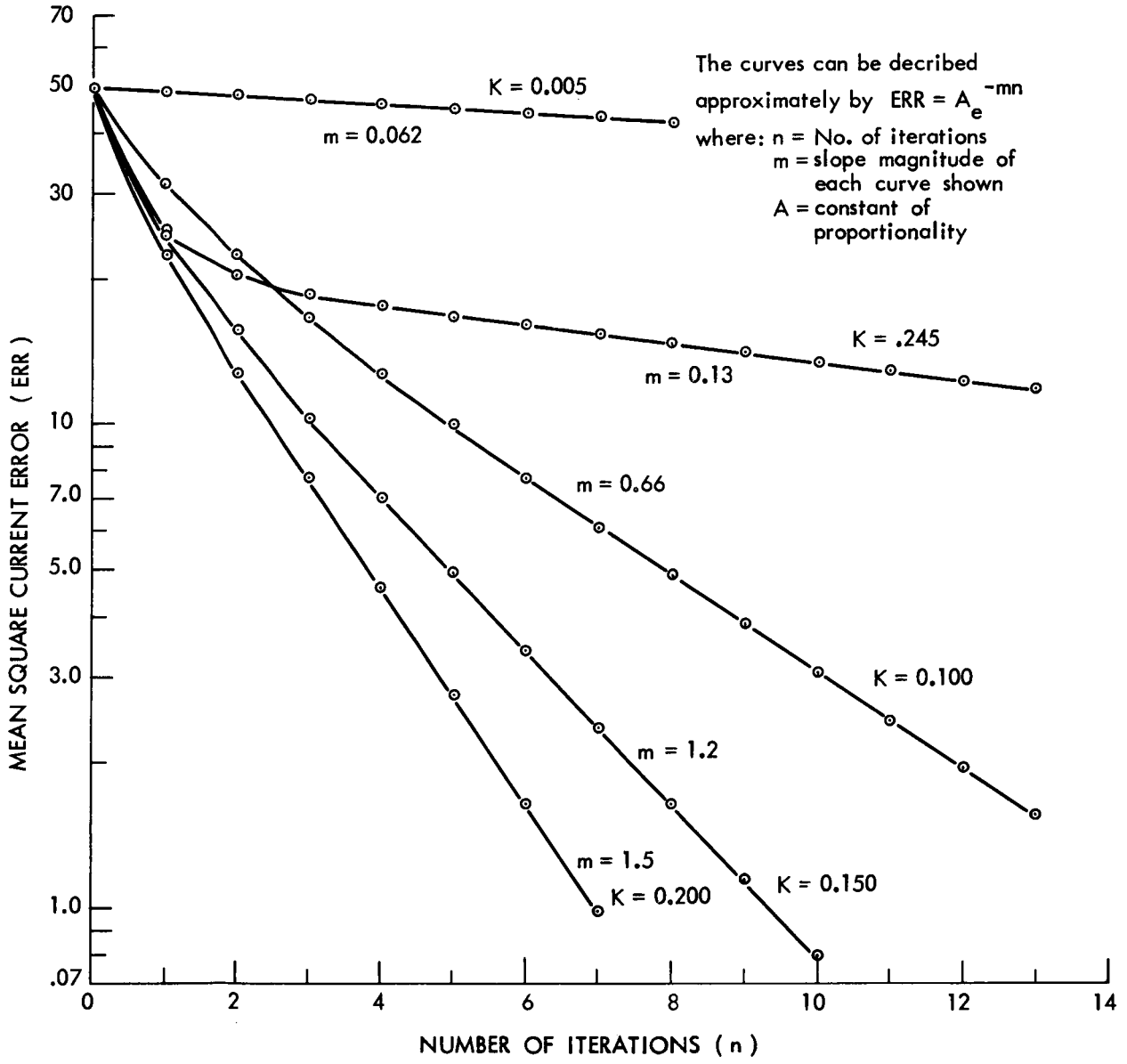


Fig. 2 MEAN-SQUARE CURRENT ERROR vs ITERATION NUMBER WITH PARAMETER K

III. SYNTHESIS OF LOGIC CIRCUITS

Professor M. L. Dertouzos
Mr. Paul J. Santos -
Research Assistant

This problem of logic-circuit synthesis is concerned with the design of combinatorial digital networks that mechanize any given binary input-output function, where the permissible building blocks belong to a given class. For example, a typical design problem might be to synthesize a given five-variable input-output binary function using only three-input NOR gates and building blocks, the output of which is specified by a table of combinations.

A number of design procedures already exist that perform logical design for a specified class of building blocks. Examples of this are AND-OR synthesis, NAND synthesis, and so forth. The problem of developing a suitable, fully algorithmic procedure for treating any given class of building blocks has not, to our knowledge, been treated. This is certainly understandable in view of the large number of possible one-to-many decompositions. These difficulties are not eliminated in the proposed approach, but are expected to be reduced through the exploitation of a digital computer as a means of making the numerous desired combinatorial searches, and the utilization of the human in heuristic decision-making on the basis of computer results.

In greater detail, the synthesis process is visualized as follows: Preliminary specifications are introduced into the computer through either the teletypewriter or the oscilloscope. Input information consists of the given Boolean function which is to be synthesized, and a logically complete set of building blocks specified by a table of combinations for each different block. (A logically complete set is one that can realize any Boolean function.) The program undertakes a decomposition process which is essentially a recursive goal-tree procedure, which is controllable by the operator and which has flexible "goodness" and convergence criteria. For example, the "goodness" criterion might be minimality of the number of blocks, or of logic levels, or of interconnections. In general, the convergence criterion takes the form of some restriction on the decomposition process. That is, each subfunction resulting from the decomposition of a function, satisfies a statement about its nature in a stronger way than does the parent function. Such a statement

may be, for example, a reduction of the number of ONES, so that a subfunction with, say, three ZEROS and thirteen ONES is a valid subfunction of a function with twelve ZEROS and four ONES. At each decomposition stage, the program evaluates the goal, compares it to past decompositions, executes a preliminary search and informs the operator of the reduced choices open to him. The operator interacts through either the teletypewriter keyboard or through the oscilloscope light pen and makes his decision. All bookkeeping, library building, data manipulation, and certain decisions are handled by the program.

The process of computation and interaction is applied recursively until the decomposition terminates. The output information is then displayed on a cathode-ray tube in the form of a block diagram. Observe that the convergence and goodness criteria do not, in general, give rise to optimal, but rather to suboptimal solutions. This is due to the "Markovian" nature of decomposition, where decisions made at some decomposition stage are dependent on parameters belonging to that stage alone and not to the entire past history. The necessity for adhering to such a decision structure follows from the unreasonably vast computer demands imposed by a non-Markovian process.

To date, several examples for the synthesis for four-variable functions using only three-input gates (NOR, Minority) have been worked out manually, in order to increase our insight concerning the specifics and heuristics that would apply to a more general synthesis technique. The experience thus gained has been used to derive a general flow diagram for the synthesis procedure, but as yet specific details of implementation have not been completed. The basic programming language to be used in this system is the AED version of ALGOL, in agreement with other design procedures reported here. Furthermore, for some of the routine decomposition searches, machine-language will be used, since it seems to be better suited for that purpose. Consequently, considerable time has been devoted to the learning of these languages and in experimenting with trial programs. Appreciable time has been spent also on the problem of representing the necessary information within the computer. Preliminary decisions are currently being made, and it is visualized that the related facilities of the AED language will be used for this task as well. A manually conducted example, simulating the expected computer behavior, is shown below:

Problem Specifications: 1. Synthesize the four-variable Boolean function F given by the following Karnaugh map:

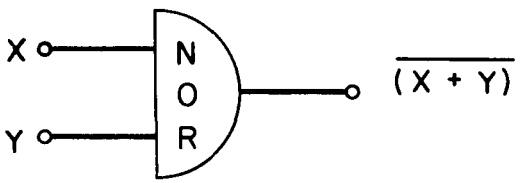
F =

CD \ AB	00	01	11	10
00	0	0	1	0
01	1	1	0	1
11	1	0	0	0
10	0	1	0	0

NOTE: 0 → ZERO
1 → ONE
ϕ → DON'T CARE

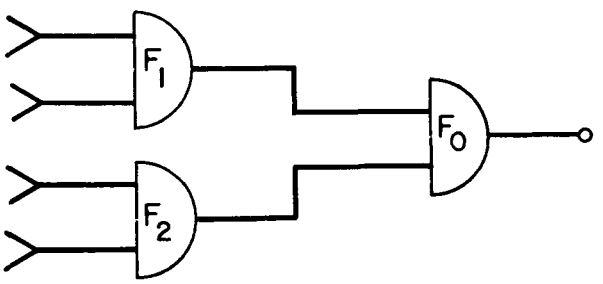
2. Use only two-input NOR gates, specified by the following Karnaugh map:

Y \ X	0	1
0	1	0
1	0	0



The input variables A, B, C, and D are available in both true and complemented form.

Synthesis Procedure: Set $F = F_o$, where F_o is the output of a NOR gate. F_o is then decomposed into F_1 and F_2 as follows:



F_1 is made independent of A and has three ONES. F_2 is dependent on all four input variables and has four ONES: F_o has six ONES. In the actual synthesis procedure, functions F_1 and F_2 were selected in the following fashion: first, an attempt was made to make F_1 the NOR of two input variables. When this failed, an attempt was made to make F_1 an input variable itself, and this failed also. The reason for these failures was the restriction that a ONE output requires all inputs to be zero which causes, in turn, both of these attempts to not "fit".

Next, an attempt was made to make F_1 independent of as many input variables as possible. This resulted in F_1 being independent of A. Since a ONE in F_1, corresponding to a ZERO in F_0, allows the corresponding place in F_2 to be a DON'T CARE, the number of ONES in F_1 was made as large as possible, consistent with the fact that the resultant function of three variables had to have less than six ONES.

The two subfunctions, F_1 and F_2 generated by the previous step are given by the following Karnaugh maps:

F_1 =

D \ BC	00	01	11	10
0	1	1	0	0
1	0	0	1	0

F_2 =

	00	01	11	10
00	ϕ	1	0	ϕ
01	0	0	1	0
11	0	ϕ	ϕ	1
10	ϕ	0	1	ϕ

Function F_1 is decomposed next into F_3 and F_4, through use of a method similar to that employed for F_1 and F_2. Now it is found that F_3 is permitted to be the NOR of C and $\overline{D}$, while F_4 is made independent of C. Thus,

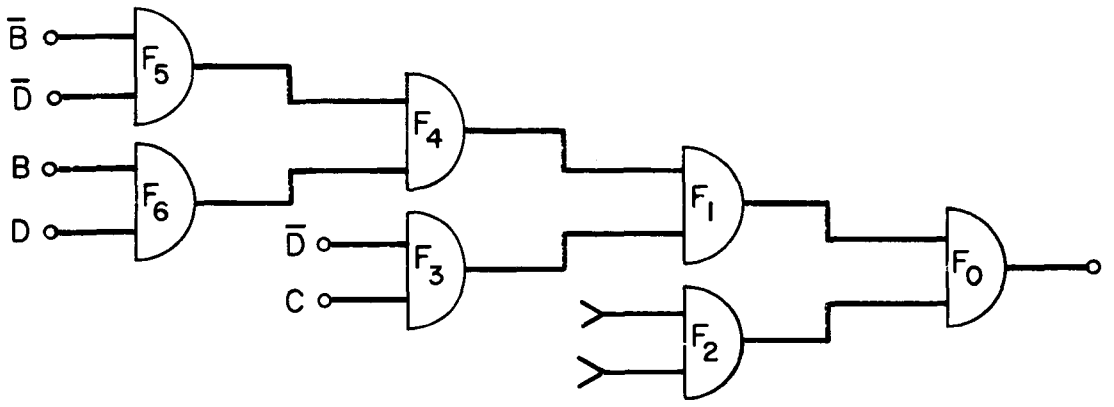
F_3 =

D \ C	0	1
0	0	0
1	1	0

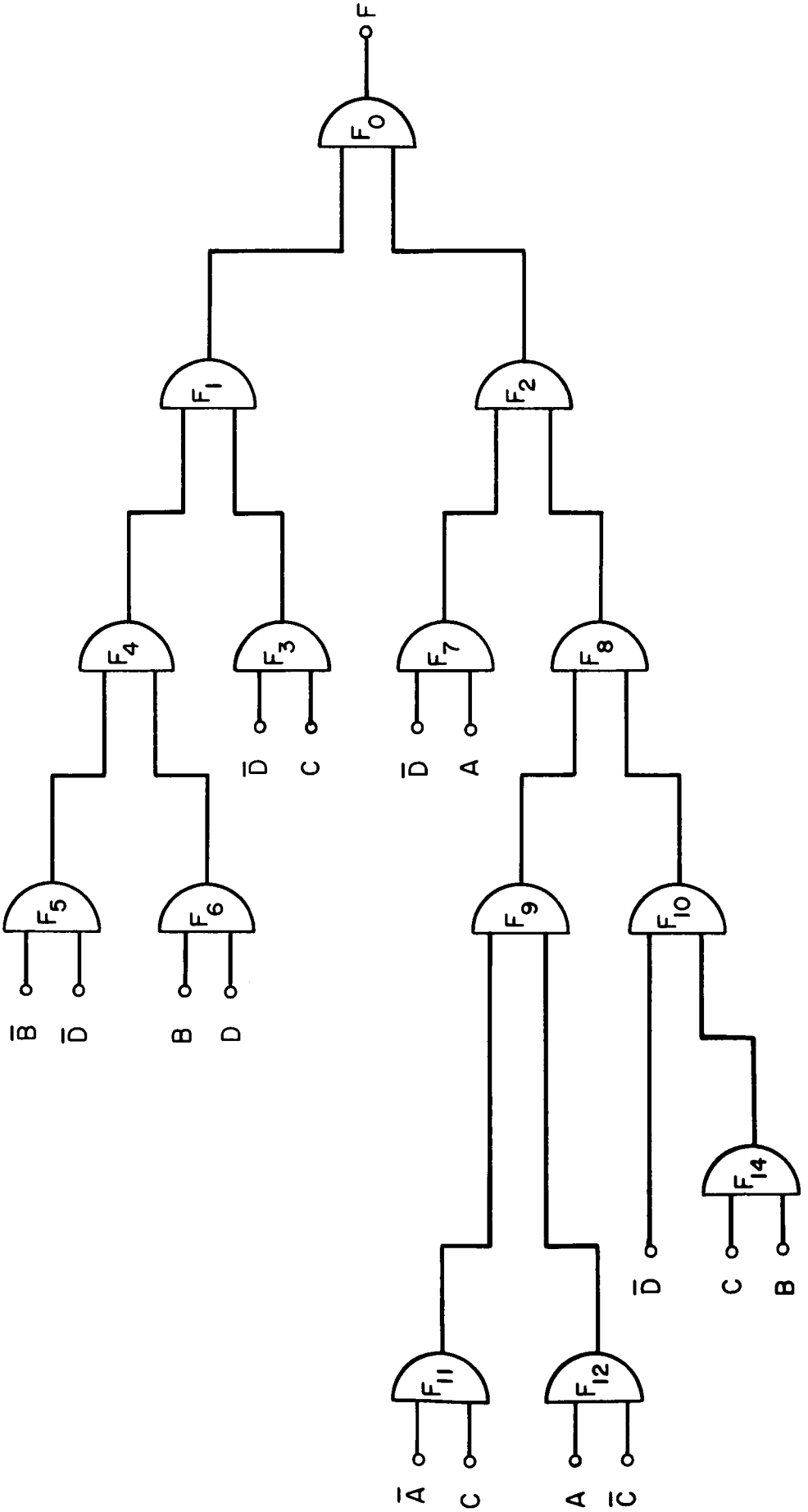
F_4 =

D \ B	0	1
0	0	1
1	1	0

F_4 is decomposed into F_5 and F_6, and F_5 is permitted to be the NOR of $\overline{B}$ and $\overline{D}$ while F_6 is the NOR of B and D. The end of this synthesis branch has been reached and consequently F_2 must be decomposed next. The partial block diagram at this stage of the synthesis is as follows:



Continuing with the synthesis, F_6 is decomposed into F_7 and F_8; F_7 is permitted to be the NOR of $\overline{D}$ and A. F_8 is decomposed into F_9 and F_{10}. F_9 is made independent of D and B and is decomposed into F_{11} and F_{12}, which are permitted to be the NOR of $\overline{A}$ and C and the NOR of A and $\overline{C}$ respectively. Thus another procedure branch terminates and now F_{10} is decomposed into F_{13} and F_{14}. F_{13} is found to be the input variable $\overline{D}$; F_{14} is found to be independent of D and the NOR of C and B. The synthesis is now terminated, since no further goals remain untackled. The final block diagram has fourteen gates and is shown on the following page.


F
F0
F1
F2
F3
F4
F5
F6
F7
F8
F9
F10
F11
F12
F14
$\bar{D}$ C
$\bar{D}$ A
$\bar{B}$ $\bar{D}$
B D
$\bar{A}$ C
A $\bar{C}$
$\bar{D}$
C B

IV. THRESHOLD LOGIC

Professor M. L. Dertouzos
Mr. Zachary Fluhr -
Fellowship Student

This work is intended to increase our understanding of logical design in terms of threshold gates. This section presents a theoretical result, concerning the behavior of a single threshold element. It is interesting to note that the validity of this result was conjectured on the basis of insight gained through man-machine interaction.

The result presented below establishes a method for finding whether a given Boolean function can or cannot be synthesized by a single threshold element. It has been already shown[1] that for any given Boolean function, G, a functional $I(\vec{c}, \vec{b})$ can be defined in terms of the characteristic vector, $\vec{b}$, of G and an arbitrary vector $\vec{c}$, such that

a. If $I_{min}(\vec{c}, \vec{b}) > 0$, the given function is <u>not realizable</u> by a single threshold element.

b. If $I_{min}(\vec{c}, \vec{b}) = 0 = I(\vec{c}_o, \vec{b})$, then the given function <u>is realizable</u> by a single threshold element, and the set of weights and threshold for that element are given by $\vec{c}_o$.

The primary difficulty, to date, has been the development of a procedure for finding the minimum of $I(\vec{c}, \vec{b})$ by adjusting $\vec{c}$. This difficulty hinges on the severe nonlinear dependence of $I(\vec{c}, \vec{b})$ on $\vec{c}$.

Our result establishes that the above functional is a <u>convex function</u> of $\vec{c}$. Hence it is possible to find its minimum, starting from any arbitrary value of $\vec{c}$, by a number of known "hill-descending" techniques. The proof of the convexity of $I(\vec{c}, \vec{b})$ follows:

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[1] The notation and results on which this development is based are presented in the following publication: M. L. Dertouzos, "Threshold Element Synthesis," Electronic Systems Laboratory Report R-200, June 1964.

$I(\vec{c}, \vec{b})$ is a convex downward function of $\vec{c}$ if and only if

$$I[\lambda \vec{c}_1 + (1-\lambda)\vec{c}_2, \vec{b}] \leq \lambda I(\vec{c}_1, \vec{b}) + (1-\lambda) I(\vec{c}_2, \vec{b}) \qquad (1)$$

where $0 \leq \lambda \leq 1$.

From the definition of $I(\vec{c}, \vec{b})$, the left side above becomes

$$\langle | \lambda \vec{c}_1 \cdot \hat{\vec{x}} + (1-\lambda)\vec{c}_2 \cdot \hat{\vec{x}} | \rangle - (\lambda \vec{c}_1 + (1-\lambda)\vec{c}_2) \cdot \vec{b} \qquad (2)$$

Using the triangle inequality, $|a + b| \leq |a| + |b|$, yields

$$\langle | \lambda \vec{c}_1 \cdot \hat{\vec{x}} + (1-\lambda)\vec{c}_2 \cdot \hat{\vec{x}} | \rangle \leq \lambda \langle | \vec{c}_1 \cdot \hat{\vec{x}} | \rangle + (1-\lambda) \langle | \vec{c}_2 \cdot \hat{\vec{x}} | \rangle$$

Substituting this inequality in Eq. 2 and rearranging yields the desired result given in Eq. 1.

Having established the desired result, we present below an example, where the realizability (or nonrealizability) of a given Boolean function is established. The "hill-descending" technique involves successive perturbations of the elements of $\vec{c}$ and retention of those perturbations that minimize $I(\vec{c}, \vec{b})$. A digital computer program was used for evaluating the functional.

A Boolean function of six variables is given (Fig. 3a) which has the following characteristic vector

$$\vec{b} = 32, 8, 8, 24, -8, 32, 0$$

Step 1

Starting with $\vec{b}$ as a first approximation for $\vec{c}$ violates the constraint $\vec{c} \cdot \hat{\vec{x}} \neq 0$. Hence c_{11} is slightly modified to yield:

$$\vec{c}_1 = 31, 8, 8, 24, -8, 32, 0$$

Computer Output: $I(\vec{c}_1) = 4$

(Observe that $\vec{b}$ is omitted from the arguments of I for convenience.)

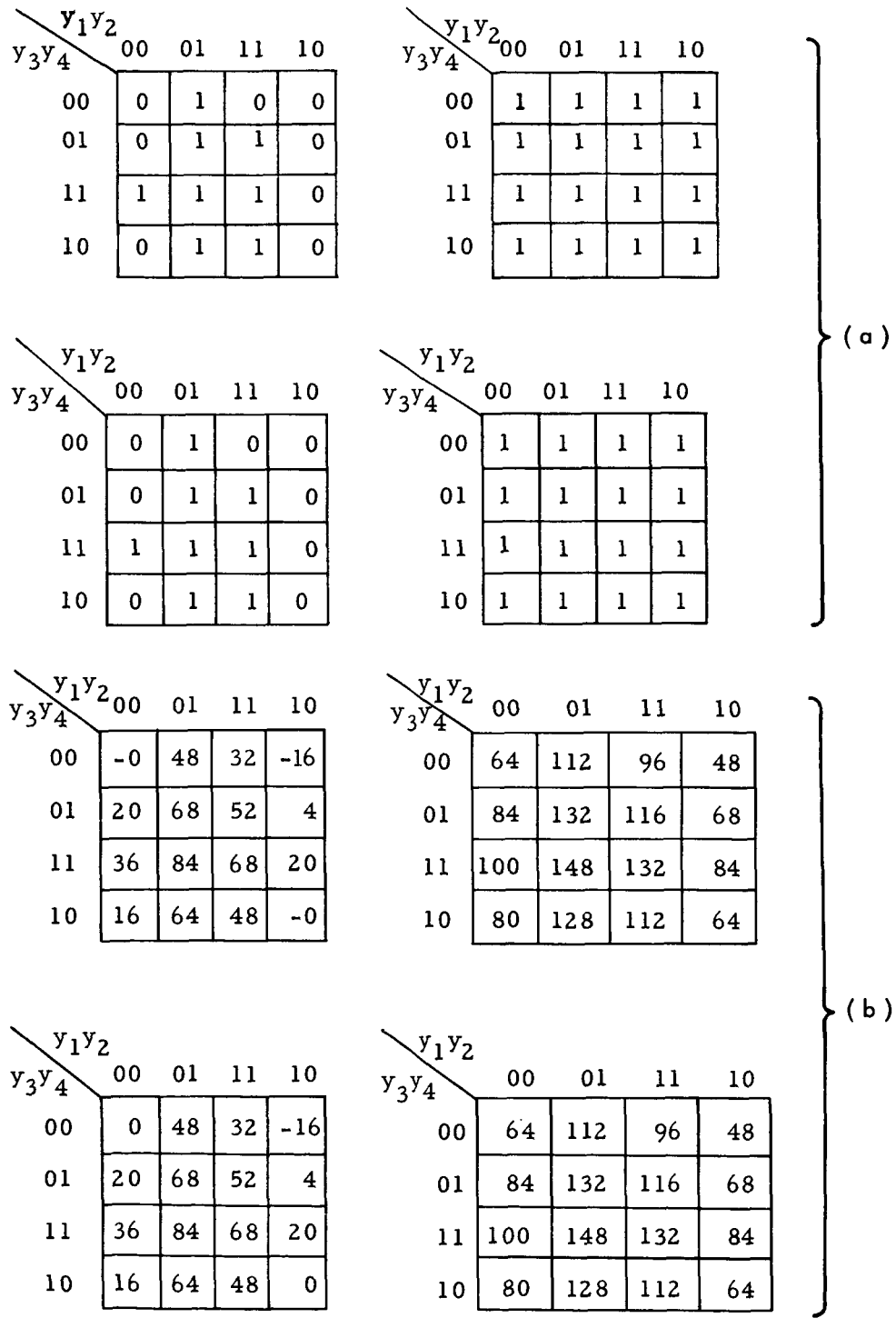


Fig. 3 EXAMPLE OF SINGLE-THRESHOLD-ELEMENT SYNTHESIS

The first element c_{11} is next perturbed by 2 units (in order to insure that $\vec{c} \cdot \hat{\vec{x}} \neq 0.$) Thus,

Step 2

$$\vec{c}_2 = 29, 8, 8, 24, -8, 32, 0$$

Computer Output: $I(\vec{c}_2) = 12$

Since $I(\vec{c}_2) > I(\vec{c}_1)$, the direction of perturbation is reversed resulting in

Step 3

$$\vec{c}_3 = 33, 8, 8, 24, -8, 32, 0$$

Computer Output: $I(\vec{c}_3) = 4$

Increasing c_{11} further, yields

Step 4

$$\vec{c}_4 = 35, 8, 8, 24, -8, 32, 0$$

Computer Output: $I(\vec{c}_4) = 12$

Hence we settle for c_{11} unperturbed and proceed with c_{12}.

Step 5

$$\vec{c}_5 = 31, 6, 8, 24, -8, 32, 0$$

Computer Output: $I(\vec{c}_5) = 16$

Reversing the direction of perturbation of c_{12} leads to

Step 6

$$\vec{c}_6 = 31, 10, 8, 24, -8, 32, 0$$

Computer Output: $I(\vec{c}_6) = 0$

Hence the iteration process terminates and it is concluded that the given Boolean function is realizable by a single Threshold Element with a weight-threshold vector $\vec{c}_6$. The weighted sums in a 0, 1 configuration corresponding to $\vec{c}_6$ is given in Fig. 3b.

PART II

CONDUCTION PROCESSES IN THIN FILMS

CONTENTS

LIST OF FIGURES

I. INTRODUCTION

This is the first semi-annual status report on Part II of the grant made to Electronic Systems Laboratory, Massachusetts Institute of Technology, by the NASA Office of Advanced Research and Technology. This grant is included for contractual purposes in NASA grant NsG-496(Part) to M.I.T.'s Space Research Center.

Part I of the grant pertains to computer-aided design of electronic circuits and is reported on in the fore part of this report.

The object of this work is to investigate conduction processes in thin insulating films. The work to date has been confined to cadium sulfide (CdS) films and to structure of gold electrode films.

The following staff has participated in the work during the past six-month period:

Dr. James G. Gottling, Assistant Professor of Electrical Engineering

Mr. W. Stewart Nicol, Staff Member

Mr. A.A. Aponick, Research Assistant

Mr. M. Cooper, Graduate Student

Mr. Walter Gajda, Graduate Student

Mr. H. Jenssen, Senior Thesis Student

Mr. M. Oliver, Senior Thesis Student

Mr. Michael Blaho, Technician

II. SURFACE-STRUCTURE STUDIES

The electron microscope facility of the M.I.T. Materials Science Center has been utilized to examine the surface structure of cadmium sulfide films. Also the structure of gold films, deposited onto cadmium sulfide as a substrate, has been examined. / A purpose of this work is to relate conduction characteristics of cadmium sulfide films to the film structure and, in turn, to the deposition technique. Another is to classify the effect that various deposition parameter combinations have upon gold structures on cadmium sulfide as a substrate. Here the goal is to establish whether or not a grid structure can be realized with gold films. Natural structural tendencies in these metallic films can produce a conducting layer, continuous in the plane of the film, but discontinuous in the direction normal to the plane of the film. A desirable grid structure will have apertures with mean diameters of about 200 to 2000 Å.

A. MICROSCOPE TECHNIQUE

In order to obtain high surface resolution, a slow-evaporation carbon replica technique was developed. Normal high current-pulse carbon replication is unsatisfactory because of insufficient resolution and sample damage. The new method, although time consuming, provides resolution of structural details as small as 30 Å both on vertical as well as lateral dimensions with little or no damage to the sample. The resolution is so high that evaporated gold in the cadmium sulfide surface remains embedded in the replica and can, therefore, be examined directly. Also, electron diffraction analysis can be conducted on the embedded gold. Shadowing with chromium provides information regarding the height of surface asperities in the cadmium sulfide and of the gold nuclei.

The carbon replica of the sample is obtained by evaporating carbon from a spectroscopic grade carbon rod. This rod is turned down from 3.0 mm to 1.5 mm over the last 2.5 mm of a 5 cm long rod. The narrow end is pressed by a spring against a large carbon block. The passage of current through the neck of the rod heats this region to evaporation temperature without overheating the supporting structures, the spring, or the contact electrode. Eight such sources are used in sequence to build up a 300 Å fine-grained carbon film on the substrate.

B. CADMIUM SULFIDE SURFACE TYPES

With the slow-evaporation carbon replica technique, it has been possible to obtain high-resolution electron microscope pictures of the surface of cadmium sulfide films. From these pictures we have identified four structural types which are related to the deposition parameters. The principal parameters are the rate of evaporation and the substrate temperature. The four types are described below:

1. Type I Surface: This surface is characterized by a uniform, fine-grained structure with no evidence of crystallinity (see Fig. 1). Evaporation conditions leading to formation of this surface type are high evaporation rate (400 to 500 Å per minute) and substrate at room temperature (22°C to 28°C).

2. Type II Surface: At higher substrate temperature (82 to 96°C) and lower evaporation rate a hexagonal polycrystalline structural pattern is established. Figures 2 through 5 illustrate this surface type as obtained with successively higher substrate temperature. Although the crystallite size shows only a small percentage increase (about 1000 Å in Fig. 2 to about 1250 Å in Fig. 5) the asperities--troughs between crystallites--are seen to diminish in depth markedly with increasing substrate temperature. In Fig. 2 the grains extend above the troughs by 100 Å, while in Fig. 5 the surface is much smoother and only a few asperities exceed 75 Å.

3. Type III Surface: This surface type also gives evidence of polycrystallinity. However, the crystallites are considerably larger than for Type II (see Fig. 6) and the surface is quite smooth. The substrate temperature is 110 to 130°C. Although the initial deposition rate was 500 Å per minute, because of a delay in the deposition process, which partially exhausts the source, and the higher re-evaporation rate, the film does not grow so rapidly as for lower substrate temperatures. Much of the film is grown at a rate less than 5 Å/min.

4. Type IV Surface: At higher substrate temperatures (above 130°C) the source has been exhausted of all visible cadmium sulfide. The small amount remaining, however, evaporates over a period of one or two hours, to provide the surface shown in Fig. 7. Although it was anticipated that higher substrate temperature should provide larger crystallites, there is no evidence of structure in the photograph. However, the surface is smooth.

Fig. 1 Type I CdS Surface Deposited on Unheated Glass Substrate (80,000 x)

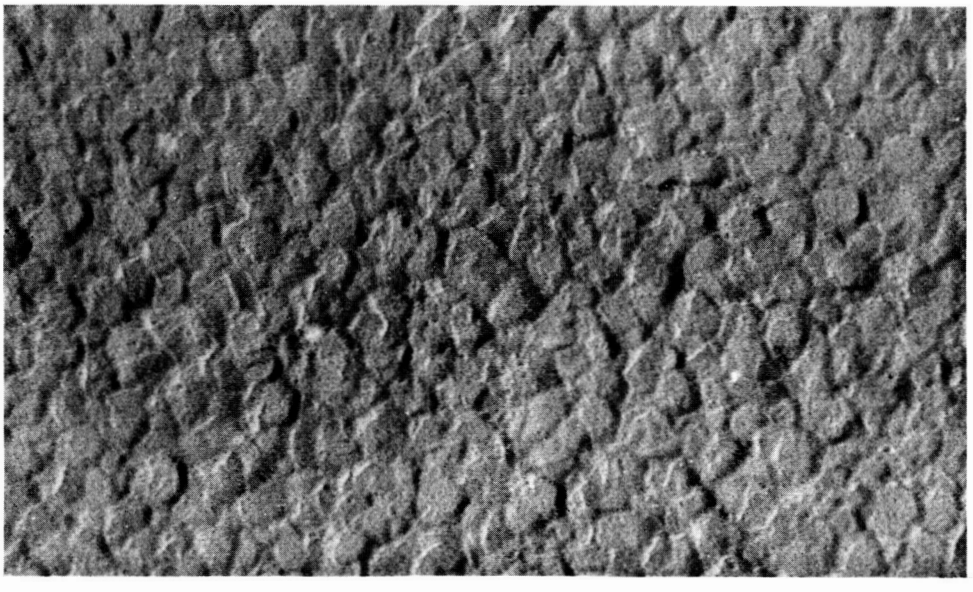


Fig. 2 Type II CdS Surface with Substrate Temperature at 83°C to 86°C (80,000 x)

Fig. 3 Type II CdS Surface with Substrate Temperature at 87°C to 90°C (80,000 x)

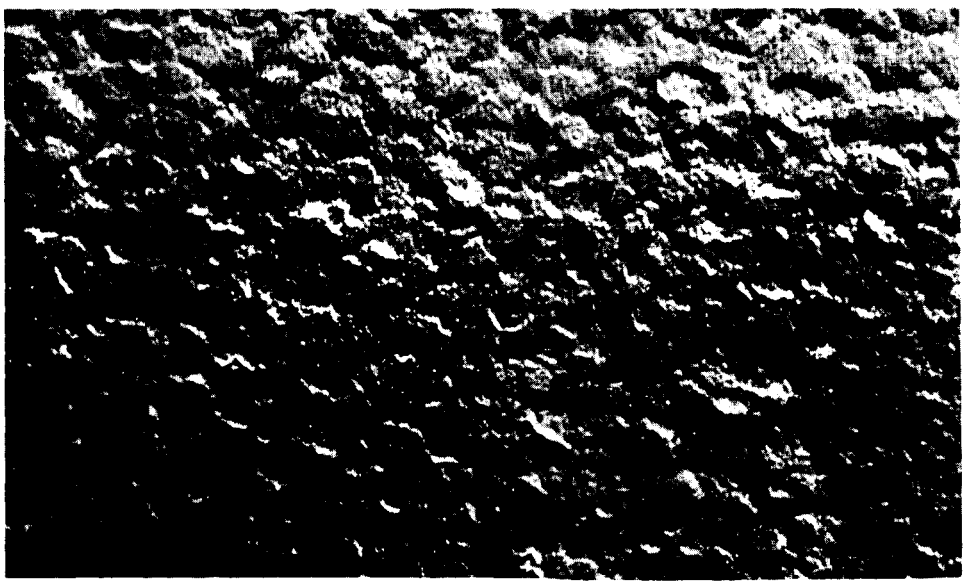


Fig. 4 Type II CdS Surface with Substrate Temperature at 88°C to 93°C (80,000 x)

Fig. 5 Type II CdS Surface with Substrate Temperature at 93°C to 96°C

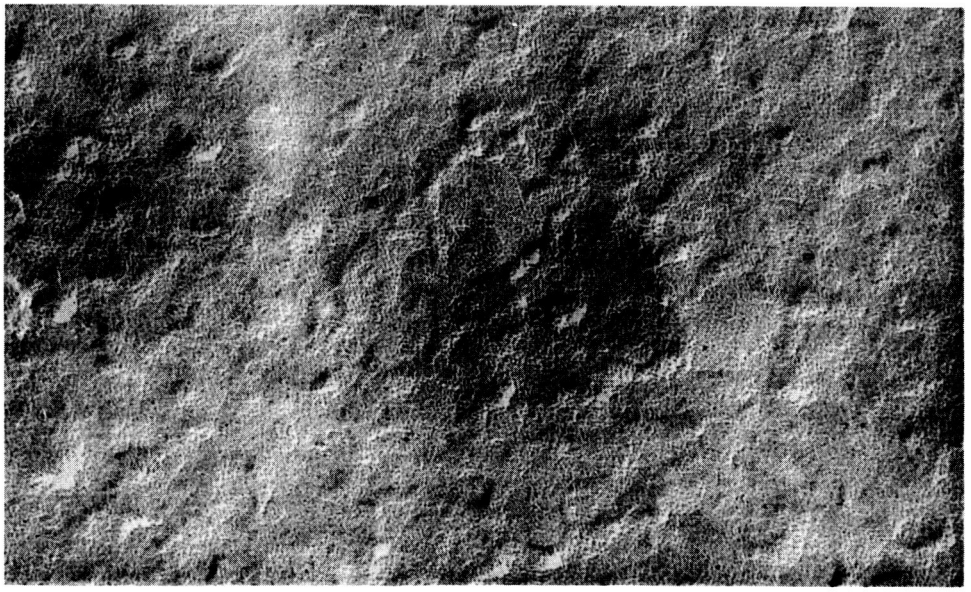


Fig. 6 Type III CdS Surface with Substrate Temperature at 123°C to 126°C (80,000 x)

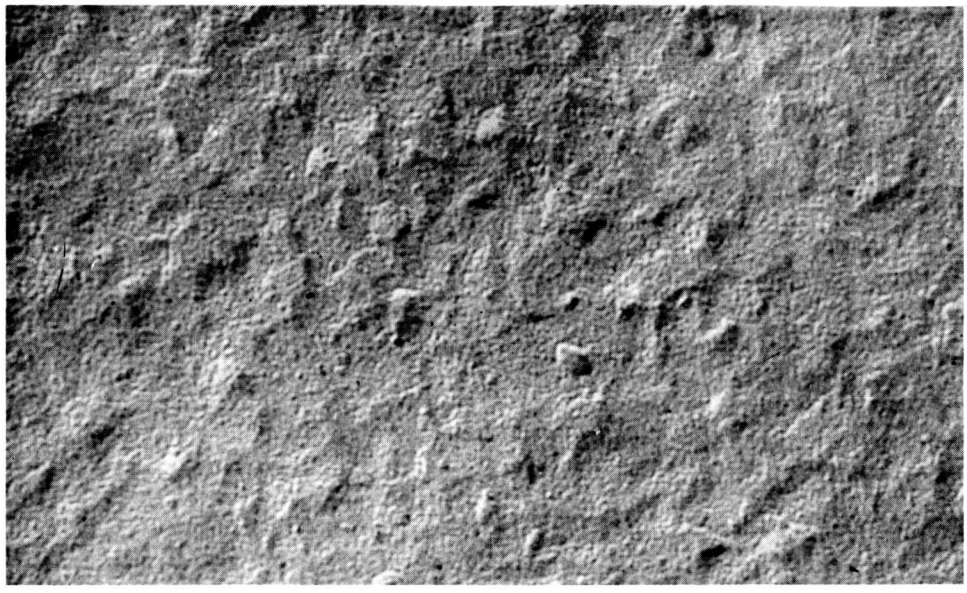


Fig. 7 Type IV CdS Surface with Substrate Temperature at 130°C to 133°C (80,000 x)

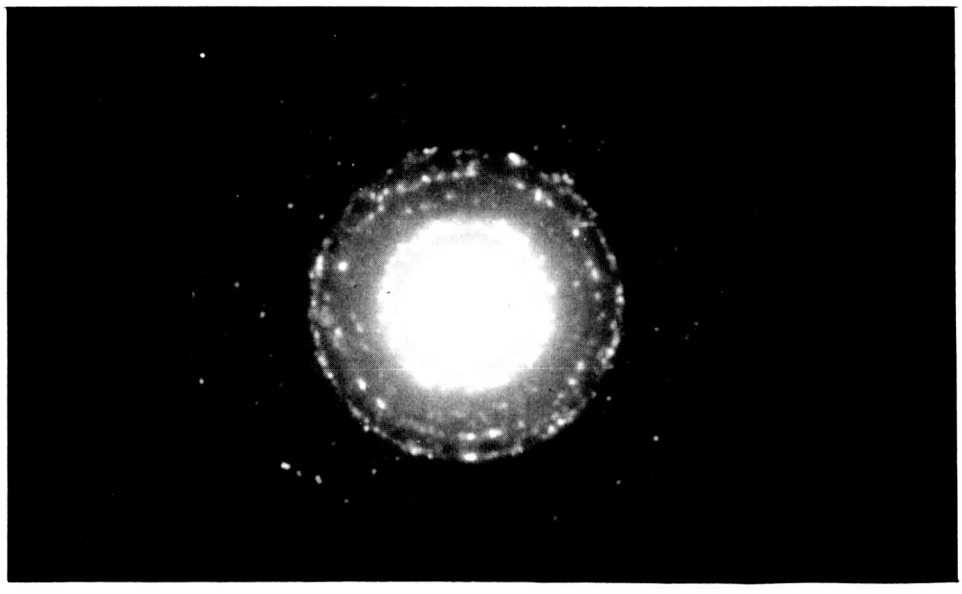


Fig. 8 Transmission Diffraction Pattern Typical of Type II, III, and IV Surfaces

The realization of these different surface types is thought to be caused by the effects produced by different combinations of substrate temperature and evaporation rate. The mobility of cadmium, sulfur, or cadmium sulfide on the substrate is temperature dependent. At higher substrate temperatures the atoms can move more readily and seek out sites in crystalline orientation with underlying deposited cadmium sulfide. However, if the evaporation rate is high so that more than one monolayer arrives at the surface in the time required for a monolayer to equilibrate on the surface, then a highly disordered structure results.

A time lag before initial deposition of cadmium sulfide onto the substrate is observed. This time lag increases with substrate temperature, and it has a value of less than a minute at 82°C which increase to 2 minutes at 93°C. Other factors which affect the time lag are surface cleanliness, evaporation rate, and exposure of the substrate to light. The mechanism for this effect is not understood, although we believe it is related to an interaction between evaporation rate and re-evaporation from the substrate.

Electron diffraction observation of the cadmium sulfide surface types was conducted by partially etching the cadmium sulfide on the carbon replica. In this way the polycrystalline portions of the film which protrude above the troughs are left in the carbon replica. Figure 8 is a transmission electron diffraction pattern typical for Type II, III and IV surfaces. Although the electron microscope photograph of Type IV surfaces does not indicate the presence of crystallites, the electron diffraction measurements indicate their presence. The beaded nature of the pattern implies that the surface contains crystallites. Because the data are for transmission diffraction, the presence of all resolvable rings associated with the wurtzite structure implies the lack of crystalline orientation.

Table I
Electron Diffraction Data for a Typical CdS Surface (Type II, III, or IV)--Wurtzite Structure

Ring	Spacing	Orientation	ASTM Spacing*
1	3.613 Å	(100)	3.583 Å
2	3.357	(002)	3.357
3	3.150	(101)	3.160
4	2.559	(102)	2.450
5	2.048	(110)	2.068
6	1.862	(103)	1.898
7	1.781	(200)	1.791
8	1.706	(112)	1.761
9	1.575	(202)	1.581
10	1.365	(203)	1.398
11	1.280	(114)	1.308

* "X-Ray Powder Data File," ASTM Publication 48L

C. DEPOSITION OF GOLD ON CdS SUBSTRATES

Using a "combination" specimen technique, we have been able to investigate the structures of small surface mass densities of gold deposited onto the various CdS surface types. A combination specimen is simply a replica of the CdS-gold surface to which the gold remains adhered after dissolution of the CdS.

A deposited surface density of 2.74 $\mu g/cm^2$ was expected to "decorate" any preferential nucleation sites on the CdS surface without interference from any structural tendencies of the gold. It was found (see Fig. 9) that such nucleation sites are very closely and uniformly distributed over the Type II surface. The Type IV surface was found to have a similar number and density of sites, but these sites do not bind the gold as strongly to the surface.

Such a distribution of sites causes the gold to form an almost solid layer when high (15 $\mu g/cm^2$) surface mass densities are deposited. We have been able to eliminate the solid-layer problem by thermally cycling the CdS-coated substrate both during and after deposition of the gold. An increase of the substrate temperature reduces the "tightness" with which the gold is bound to the surface--gold nuclei become sufficiently mobile to coalesce. In Fig. 10, 2.74 $\mu g/cm^2$ of gold was heated to 105°C for 90 minutes after deposition on a Type II surface. This annealing has increased the average grain size from 25 Å in Fig. 9 to 150 Å here.

Fig. 9 2.74 μgrams-cm^{-2} Au Decoration Sites on Type II CdS

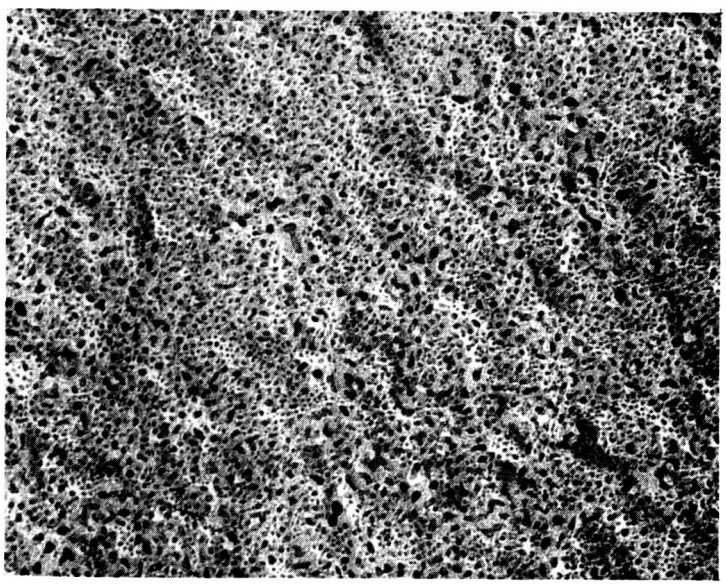


Fig. 10 2.74 μgrams-cm^{-2} Au on Type II CdS Annealed to 105°C for 90 minutes

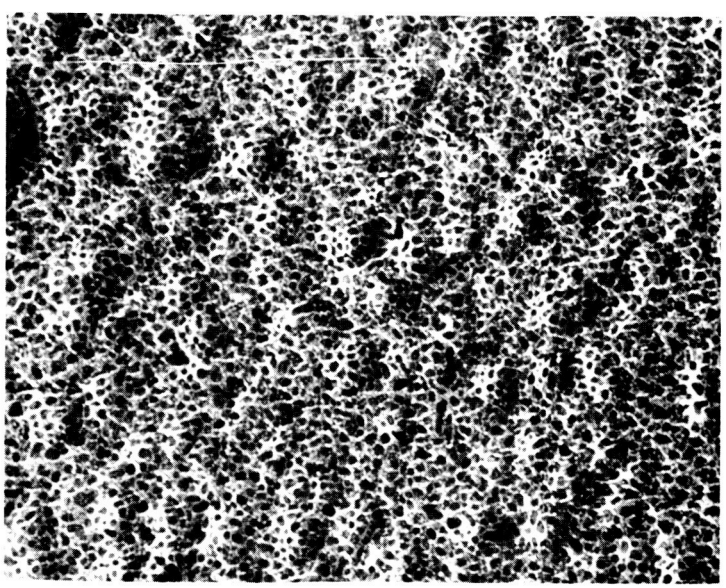


Fig. 11 8.23 μgrams-cm^{-2} Au on Type II CdS

We have found that as the surface mass density of the gold is increased, coalescence can be made to occur again and again at elevated substrate temperatures, and a grainy structure is maintained up to densities of 8.23 $\mu g/cm^2$ (see Fig. 11). Low deposition rates and high substrate temperatures maintain the graining structure, but post-deposition annealing was found to have an even greater effect on granularity than heating during deposition. It is presently thought that these same techniques can be used on yet higher surface mass densities of gold, and that at some critical density coalescence will occur between grains sufficiently large to make the film electrically continuous, but of a lacy, grid-like structure. Work toward the fabrication of this structure is now in progress.

III. CONDUCTIVITY OF THIN-FILM CADMIUM SULFIDE

Cadmium sulfide is well-suited to application as a conducting medium in thin film active circuits, where device performance occurs uniformly in a direction normal to the substrate. Most conducting materials cannot provide high enough resistance to the flow of current. Although it is an insulator, ohmic contact from suitable metal film electrodes can introduce injected currents. For these reasons we have been measuring the conductivity characteristics of such films.

A. FABRICATION OF THE DIODES

The thin-film cadmium sulfide diodes are prepared by vacuum evaporation from an electrically heated, refractory metal source. Although molybdenum ribbon sources have been used, future work will make use of a quartz crucible source to eliminate possible chemical reaction of the cadmium sulfide with the heated source. A routine cleansing process is applied to the substrate to assure clean deposition surfaces. Both heat treatment and glow discharge during pump-down are also employed to clean the surface. The diodes have gold metal electrodes on both top and bottom surfaces, so that a gold film is first deposited onto the substrate. The subsequent deposition of the cadmium sulfide occurs for a period of time ranging from about five minutes up to an hour. During this time the substrate temperature is maintained essentially constant at a value ranging from ambient up to 250°C. The evaporation rate is typically 400 to 500 $\mathring{A}$ per minute. Before deposition of the top gold electrode, the upper surface of the cadmium sulfide film is exposed to a glow discharge bombardment of argon atoms at 50 μHg pressure and 1500 to 2000 volts. Although this bombardment has been proposed as a technique to assure ohmic contact, we have found that diodes formed in this manner produce rectification characteristics which correspond to the assumption that the upper gold electrode forms the more blocking contact.

B. DARK CONDUCTIVITY OF Au-CdS-Au DIODES

The dependence of current through a typical diode, upon the temperature with no light applied to the device, is shown in Fig. 12. Here the logarithm of the current is plotted vs. $\frac{1}{T}$. The data are taken after reducing the temperature,

and the temperature of the sample is raised during the readings at a slow rate ($\cong 0.05^{o}K/sec.$). When data are taken during quenching, the current at any temperature is lower than the value observed during the rising temperature. Also, the exponential variation of current with reciprocal temperature does not occur. This effect is believed to be caused by trapping of electrons, which results from their inability to be withdrawn from the CdS due to surface barrier layers at the gold contacts. This trapped population of electrons then produces a space charge within the film which further reduces the emission current. Not all devices demonstrate the exponential result shown in Fig. 12. Those that do not are more conductive than film No. 188 at high temperature values, and these films are notably poor rectifiers.

In order to interpret the data of Fig. 12, we have utilized Fermi-level analysis. Assuming that the applied voltage is distributed uniformly across the width of the film and neglecting temperature variation of mobility and effective density of states

$$\frac{i}{A} = \sigma\left(\frac{V}{t}\right) = (n q \mu)\,\frac{V}{t} = q N_c \mu \left(\frac{V}{t}\right) \exp\left[\frac{E_f - E_c}{kT}\right] \qquad (1)$$

or

$$E_f = E_c + kT \ln\left[\frac{ti}{qN_c \mu V A}\right] \qquad (2)$$

where

i = total current

σ = conductivity

n = majority carrier concentration

q = electronic charge

μ = electron mobility $\cong 4\ cm^2/volt\text{-}sec.$

N_c = effective density of states in the conduction band, $qN_c = 1.6\ coulomb/cm^3$

A = diode area $\cong 10^{-2}\ cm^2$

t = CdS thickness = 4800 Å

V = applied voltage = 1.8×10^{-2} volt

E_f = Fermi-level energy

E_c = conduction band energy

k = the Boltzmann constant

T = absolute temperature

Although the value of N_c might be changed to include the effective mass of conduction electrons in CdS ($0.2\ m_o$), and there is some doubt regarding the value of the electron mobility, nevertheless large changes in the argument of the natural log expression do not produce appreciable changes of the value of E_f. For the indicated numerical values

$$E_f = E_c + kT \ln(0.0417\ i) \tag{3}$$

The data of Fig. 12 are used with Eq. 3 to obtain the plot shown in Fig. 13. The portion of the Fermi-level curve labeled "A" in this figure extrapolates to the value of the conduction band energy at zero temperature. This region can be interpreted as due to a shallow level of donors, which in this range of temperature are completely ionized. Then

$$E_f = E_c - kT \ln \frac{N_d}{N_c} \tag{4}$$

Because of the possibility that deeper-lying traps are completely filled at this temperature, N_d in Eq. 4 has to be interpreted as the excess of shallow donors over the number of deeper-lying traps. From the slope of the curve in Fig. 13, the value of N_d is

$$N_d \cong 10^{12}\ cm^3 \tag{5}$$

The portion of the curve, labeled "B", is a straight line which has a value of $-0.05\ eV$ when extrapolated to zero temperature. One might be tempted to conclude that this extrapolated value represents half the energy of a shallow donor level, since for such a level

$$E_f \cong \frac{E_c + E_d}{2} - \frac{kT}{2} \ln \frac{2N_c}{N_d} \tag{6}$$

However, this equation is only applicable when the Fermi level is already above the donor level, so that the donors are only partially ionized. This condition is not applicable here for the numerical values assumed. In order to obtain values of E_f, which are consistent with partially ionized donors, the value of $(q N_c \mu VA)$ must be decreased or (ti) must be increased. We assume that this conduction is associated with a much smaller area than the

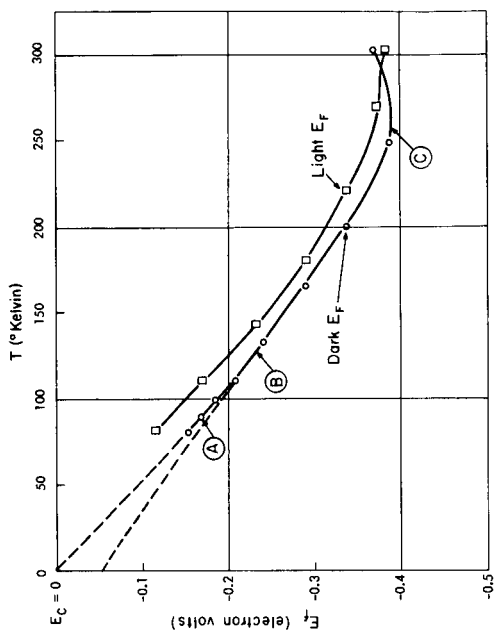


Fig. 13 Fermi Level vs. Temperature

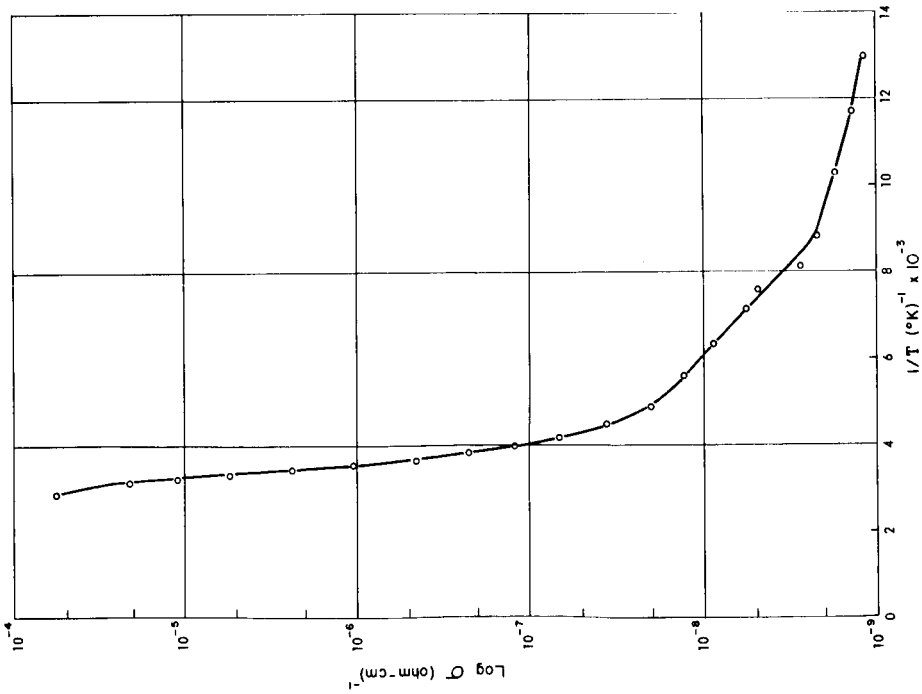


Fig. 12 Variation of CdS Film Conductivity with Temperature (Dark)

apparent area of the diode. Then the effective area for conduction is about 7 orders of magnitude smaller than the apparent area in order to obtain E_f values greater than -0.1 electron volt. This conduction appears to be associated with a surface phenomenon, as might be the case if crystallite surfaces within the CdS film were conducting. Since the exact slope is not known with certainty, but the area is estimated to be 10^{-9} cm^2, we recalculate the donor density from the data of Fig. 12 where

$$i \cong 5 \times 10^{-9} \text{ to } 8.6 \times 10^{-7} \text{ amp} \tag{7}$$

When the donors are saturated, with no excitation from traps,

$$i = N_d q \mu V A/t \tag{8}$$

With the area A equal to 10^{-9} cm^2 and all other parameters remaining as before, we now have

$$N_d \cong 10^{16} \text{ to } 10^{18} \text{ cm}^{-3} \tag{9}$$

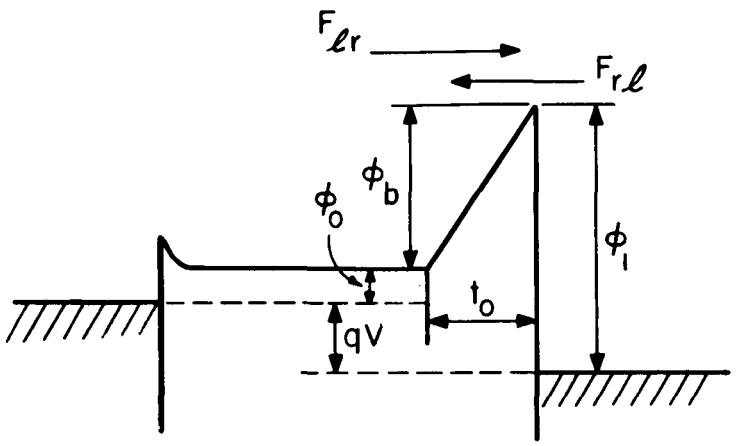
The uncertainty is caused by the fact that the current increases exponentially with a gap of 0.59 eV due to the parallel conduction process. Thus the donor saturation value is not observed.

The curve at high temperature, labeled "C" in Fig. 12, appears not to be described by a Fermi-level analysis. The slope of this portion of the characteristic in Fig. 12 indicates an energy of 0.59 electron volt. We believe that this slope is a measure of the height of the barrier between the top metal electrode and the CdS. The current is believed to be limited by Schottky emission. The expression for Schottky emission corresponding to the energy barrier of Fig. 14 is

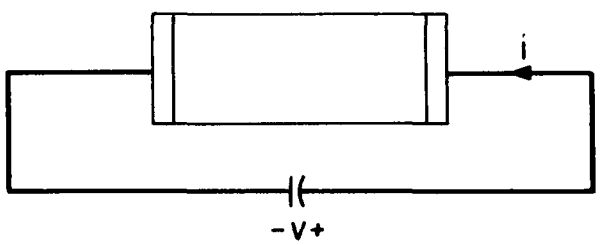
$$J = ST^2 \left[\exp - \frac{\phi_1 - \Delta\phi}{kT}\right] \left[\exp\left(\frac{qV}{kT}\right) - 1\right] \tag{10}$$

where Richardson's constant is

$$S = (1-r)\, 4\pi q m k^2/h^3 = 120\,(1-r) \text{ amp/cm}^2/{}^{o}\text{K}^2 \tag{11}$$



(a) Electron Energy Diagram (not including image force energy)



(b) Polarity Definitions for the Diode

Fig. 14 Linear Approximation to Electron Energy in CdS Diode

and

$$\Delta\phi = \sqrt{qE/4\pi\epsilon} = \sqrt{\frac{14.3E}{\kappa}} \quad \text{electron volts} \tag{12}$$

Here, κ is the relative dielectric constant of the CdS. The electric field is

$$\overset{o}{E} = \frac{(\phi_b/q) - V}{\overset{o}{t}_o} \tag{13}$$

where $\overset{o}{E}$ is the electric field in volts/$\overset{o}{\text{A}}$ngstrom within the blocking region of the upper gold electrode - CdS contact and κ is the relative dielectric constant of the CdS. In the temperature region of Fig. 12 where the current varies exponentially as -0.59/kT

$$i = 1.1 \times 10^{5} \exp -(0.59/kT) \tag{14}$$

If we take

$$t_o = 500 \text{ Å} \tag{15}$$

$$\phi_b \tilde{=} \phi_1 \tilde{=} 0.59 \text{ electron volt} \tag{16}$$

$$\epsilon = 11$$

then

$$\Delta\phi \tilde{=} 0.04 \text{ electron volt} \tag{18}$$

Consequently, the height of the barrier between the top gold electrode and the conduction band in the CdS appears to be

$$\phi_1 = 0.63 \text{ electron volt} \tag{19}$$

With

$$V = -18 \text{ millivolts} \tag{20}$$

changes in $T^2[\exp(qV/kT)-1]$ can be neglected because at low voltage this term does not change rapidly with the temperature compared to the exponential factor involving the barrier height. Then, for the Richardson constant, the experimental data gives

$$S = 256 \text{ amp cm}^{-2}\,{}^{o}\text{K}^{-2} \tag{21}$$

Although this value is larger than the accepted value (120 amp $\text{cm}^{-2}\,{}^{o}\text{K}^{-2}$), and we might expect a smaller value due to nonzero reflection coefficient, a higher value can be justified for emission from a metal well above the Fermi level due to an increased effective mass. The above experimental value agrees with the accepted value as an order-of-magnitude calculation, and we, therefore, believe that these calculations strongly suggest that the higher temperature portion of the data in Fig. 12 is caused by Schottky emission.

C. VOLTAGE DEPENDENCE OF DIODE CURRENT

The current as a function of voltage for a typical thin-film CdS diode is shown in Fig. 15. These measurements are for a temperature of 90^{o}K.

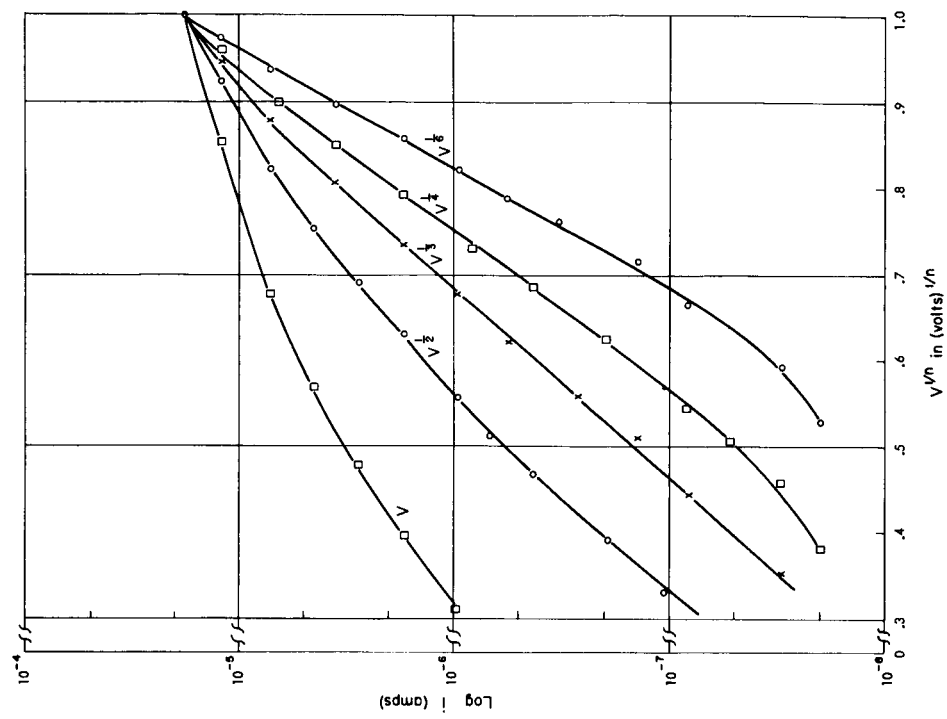


Fig. 16 CdS Diode Reverse Current vs. $V^{1/n}$

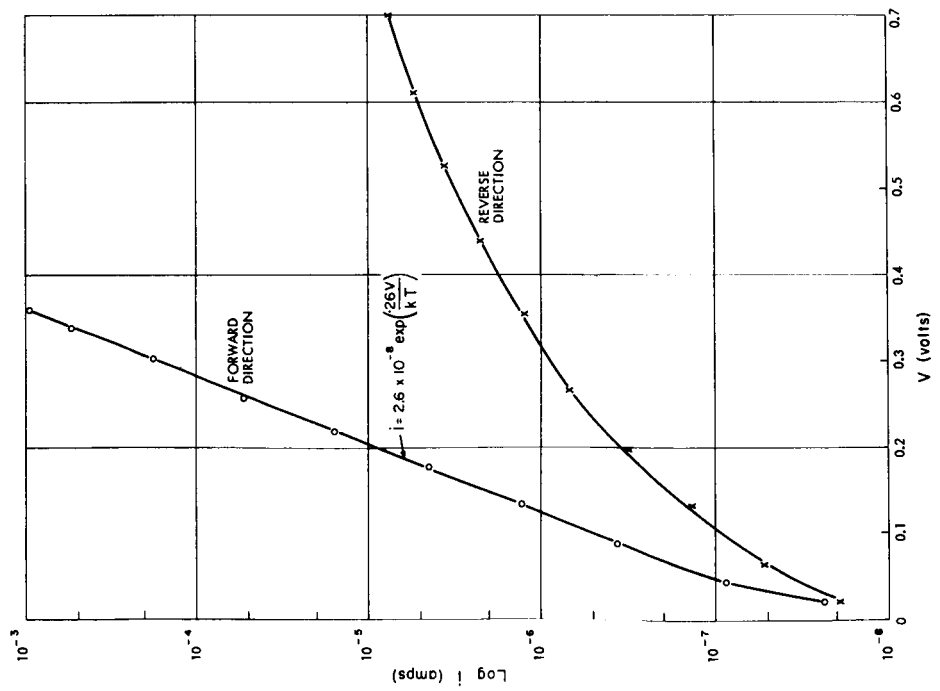


Fig. 15 CdS Diode Current vs. Voltage (102°C)

The forward current characteristic (top Au electrode positive) varies exponentially with voltage. This result is expected if the current is emission limited, since at more than 10 millivolts forward bias the exponential term in Eq. 10 will provide the dominant variation with voltage. However, the slope of the experimental data (31.8 nepers per volt) is smaller than the expected value (120 nepers per volt). This discrepancy is a defect in the Schottky emission model proposed above. A more serious deficiency is evident in the reverse bias characteristics. Here (see Fig. 16), although the curves plot as straight lines with $V^{1/n}$ as abscissa (n = 4 or 6), this result is not consistent with the simple theory. If the barrier thickness is assumed to vary as the square-root of the field, the 1/4 power dependence results. Alternately, if a quadratic potential variation is assumed and the Schottky lowering of the barrier is computed--again with voltage dependent thickness--the 1/6 power law results. However, with a built-in field $(\phi_1 - \phi_o)/qt_o$ at zero bias, the slope of the reverse bias curve should not become linear until the applied voltage is comparable to the built-in potential difference. Since the curves are linear below 0.3 to 0.4 volt, the experimental data do not conform to the model where a built-in field occurs at the metal contact.

IV. THERMALLY STIMULATED EMISSION CURRENT

If a semi-insulating material at low temperature containing traps is exposed to optical excitation by light with sufficiently long wavelength, then when the temperature is raised, more current flows than for the case with no optical excitation. This difference is due to optical excitation of electrons from the valence band to the conduction band followed by condensation into the traps. The thermally-stimulated current is a measure of the location of the traps in the forbidden gap and may also provide a measure of their density.

For an insulator having constant concentration of carriers per unit volume in the dark along a lateral dimension, excitation by light at low temperatures raises the Fermi level for electrons. At any temperature thereafter the number of carriers in the conduction band is

$$n = N_c \exp - [E_c - E_f]/kT \tag{22}$$

The measured current after stimulation is

$$I_s = \frac{q \mu n A V}{t} \tag{23}$$

Solving for the Fermi level

$$E_f = E_c - kT \ell n \frac{qN_c \mu A V}{I_s t} \tag{24}$$

This equation then is used to evaluate E_f when the difference between the light and dark current (I_D) is a maximum. If we assume that I_D is a maximum when the Fermi level is at the level of the traps, then the level of the trap measured from the edge of the conduction band is obtained.

The thermally stimulated current I_D for a typical CdS film is shown in Fig. 17. Two distinct peaks occur. The peak at low temperature corresponds to a level only 0.116 eV below the conduction band. The second peak is produced by a level 0.372 eV below the conduction band. We believe that the peak at a shallow level is associated with shallow donors (sulfur deficiency) which at normal temperature are completely ionized. The peak due to the 0.372 eV level is presumed to be a normal trapping level in CdS.

The above analysis may not be applicable to our films because of the blocking contact at both Au electrodes. The following analysis is applicable when the flow of current through a semi-insulating film is limited primarily by Schottky emission at a blocking contact. In this case

$$I_D = AST^2 \exp-[(\phi_1 - \Delta\phi)/kT]\{\exp qV/kT - 1\} + I_L \qquad (25)$$

and

$$I_S = AST^2 \exp -[(\phi_1 - \Delta\phi)/kT]\{\exp \frac{qV + \Delta E_f}{kT} - 1\} + I_L \qquad (26)$$

where I_L is the leakage current in parallel with current through the barrier region and the other symbols are as previously described. Then

$$\frac{I_S - I_D}{I_D - I_L} = \frac{\exp(\frac{qV}{KT})}{[\exp(\frac{qV}{kT}) - 1]}\{\exp \frac{\Delta E_f}{kT} - 1\} \qquad (27)$$

or

$$\Delta E_f = kT \ln \{[1 - \exp -(qV/kT)](\frac{I_S - I_D}{I_D - I_L}) + 1\} \qquad (28)$$

If none of the thermally stimulated current (excess of light current over dark) is reinjected and recombination within the diode is negligible, then

$$I_S - I_D = q(\frac{\delta\Delta E_f}{\delta t}) m_t A t \qquad (29)$$

where n_t is the density of traps per unit volume and unit energy range. Equations 28 and 29 are utilized to obtain Fig. 18 where n_t is shown as a function of the distance from the edge of the conduction band. This distance is measured by assuming that ϕ_o, the energy difference between E_c and the dark Fermi level is given by

$$\phi_o = kT \ln \frac{N_c}{N_d} \qquad (30)$$

This equation results from assuming a completely ionized donor level above the Fermi level with density N_d. In the plot we have assumed N_d to be about 10^{12} per cm^3. The plot indicates a principal trapping level at -0.365 electron volt which agrees closely with the Fermi-level, conductivity method. Two minor peaks occur at -0.25 electron volt and -0.3 electron volt. However, these

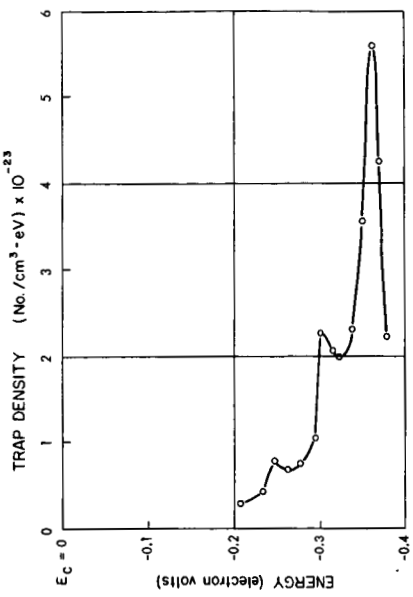


Fig. 18 Trap Density vs. Energy

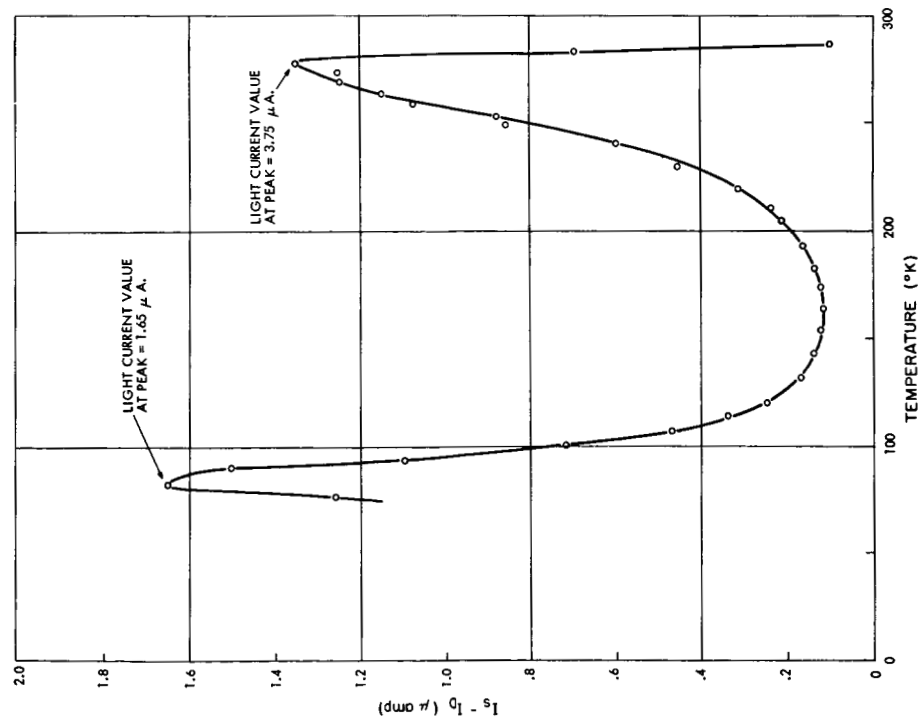


Fig. 17 Thermally Stimulated Current

may be spurious peaks produced by errors in data which are magnified when $\delta\Delta E_f/\delta t$ is evaluated. The area under the curve indicates a trapping density per unit volume of about 10^{22} which corresponds to about one trapping site per atom in the CdS film. Either the film is extremely disordered or the electrons circulate through the film more than once before suffering recombination. Then the trapping density value must be reduced in proportion to the photoconductive gain.

The above considerations may be altered considerably if part of the thermally stimulated current is due to holes. Since both contacts to the diode are blocking contacts for electron injection, presumably these are no barriers to the removal of holes from the film. However, re-injection of holes is unlikely, so that removal of holes would produce a space charge. This space charge would tend to reduce the size of the blocking potential barrier. In this case the thermally stimulated current would be larger than the dark current by more than is necessary to account for removal of electrons (or holes) from traps. These considerations provide another explanation for the high density of traps predicted by the above method.

V. DE-EXCITATION OF THIN CdS FILMS BY HIGH ELECTRIC FIELDS

A. EXPERIMENTAL WORK

The long-term decay of photoconductivity in a thin CdS film having evaporated gold electrodes has been measured for periods up to 45 hours. The film was first cooled in darkness from room temperature to 90°K, the current density then decreasing to a steady value of 1.35×10^{-10} amp/cm^2 with an applied direct field of 4×10^2 volt/cm. It took approximately one hour to reach this steady value. The film was then optically excited with white light for two minutes during which time the current density rose to 5.8×10^{-7} amp/cm^2. Forty-five seconds after the excitation, the current decay was found to obey the inverse relation $i \sim t^{-\alpha}$ where

$$\alpha = 0.73 \qquad (45 \text{ sec} \leq t < 2 \text{ min})$$
$$\alpha = 0.40 \qquad (2 \text{ min} \leq t < 5 \text{ min})$$
$$\alpha = 0.23 \qquad (5 \text{ min} \leq t < 65 \text{ min})$$

Between 65 and 1200 min the decay rate decreased steadily, increasing again between 200 and 500 min. At t = 500 min. when the current density had fallen to 7×10^{-9} amp/cm^2, the applied field was removed. From 500 min. to 1,330 min. there was no applied field and no decay. At 1,330 min. the field was again applied and the decay continued, the current density falling to 2×10^{-9} amp cm^{-2}, 45 hours after the excitation.

A second CdS film was allowed to decay with the same applied field (4×10^2 volts cm^{-1}), following two minutes optical excitation with white light, during which the steady current density was 10^{-6} amp cm^{-2}. The inverse relation $i \sim t^{-\alpha}$ again held, where

$$\alpha = 0.76 \qquad (1 \leq t < 2 \text{ min})$$
$$\alpha = 0.62 \qquad (2 \leq t < 4 \text{ min})$$
$$\alpha = 0.2 \qquad (t \geq 4 \text{ min})$$

Thirty-six minutes after excitation, when the current density had decayed to 4×10^{-8} amp cm^{-2}, the applied field was increased to 0.8×10^5 volt cm^{-1} for two seconds. Following this, the steady current density dropped to 5×10^{-9} amp cm^{-2}. Later, when the current density had decayed to 2.5×10^{-9} amp cm^{-2}, the high field (0.8×10^5 volt cm^{-1}) applied for two seconds with the opposite polarity, resulted in a fall in current density to 5×10^{-10} amp cm^{-2}.

B. PRELIMINARY CONCLUSIONS

From these and other experiments, the following points are noted:

1. The decay of photoconductivity under a small applied field can be expressed by an inverse, t^{-a}, relationship usually associated with the presence of traps.

2. The current resulting from a small applied field can be changed by an order of magnitude by the momentary application of a high field. The magnitude and duration of this field, as well as its direction across the film, influences the change in current.

3. The long-term decay of photoconductivity is affected by the presence of even a small applied field.

4. From thermally stimulated current measurements, the film which was subjected to high field intensities, has an activation energy of 0.1 electron volt, agreeing with the 0.1 electron volt donor energy level found for these films. Using the Fowler-Nordheim relationship, the probability of tunnel emission from an energy level ΔEeV below the conduction band, under an applied field V volt cm^{-1} is given by

$$\exp - \{3.08 \times 10^7 \ \frac{\Delta E^{3/2}}{V}\} .$$

For $\Delta E = 0.1$ electron volt and $V = 10^5$ volt cm^{-1}, the emission probability is 0.39.

5. The change in Fermi level resulting from the application of high field intensities is only of the order of five percent. This small change is considered to be due to the ionization of a large number of donor atoms by the field (or due to excitation from surface states) giving rise to a space charge within the CdS film.

In addition to supplying further information about the traps in insulating film, these field excitation experiments will also yield results which may suggest possible memory device applications.

VI DISCUSSION

The structure of the evaporated CdS films (1000-4000 Å) has been observed to be polycrystalline with no preferred orientation. This observation disagrees with that of Zuleeg and Muller* where a preferred orientation of the c-axis normal to the substrate was observed for 1000 Å films obtained by vapor deposition. The size of crystallites in the evaporated films ranges from 100 to 1000 Å, depending on the substrate temperature and evaporation rate. The effect the structure has upon film conductivity is not completely determined. However, a leakage current associated with crystallite surfaces or intercrystalline material is believed to exist. Also, the possibility that crystallites do not extend throughout the film is suggested to account for voltage dependence of the forward conduction.

The observations of conduction in the CdS films with blocking Au electrodes can be accounted for by Schottky emission over a barrier about 400 to 500 Å thick. The height of the barrier at the top Au contact is about 0.6 eV and decays to 0.35 eV within the film. The concentration of donors within the CdS film appears to be about 10^{12} per cm^3 and is assumed to be caused by sulfur lattice vacancies. A principal trapping level exists at -0.36 eV to -0.38 eV; however, there is some doubt as to the density of these traps. Conduction at low voltage and low temperature can occur by an ohmic leakage process; however even with Type II CdS this leakage is sufficiently low not to interfere with device performance. The conduction with forward bias depends exponentially on qv/akT where a is about 4. This result can be accounted for if each crystallite within the film is assumed not to extend across the entire thickness of the film. Then a sequence of 4 such barriers, having the same saturation current density, equally share the applied voltage. The existence of these barriers is undesirable if these films are to be used in construction of active devices. Blocking barriers in between emitter and collector of an active device represent series voltage drops which are unrelated to the modulating process in the active device, and, therefore, deteriorate device performance. Recrystallization using a flux such as Ag, Cu, or Pb can eliminate these barriers by forming larger crystallites which extend across the film.

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* Zuleeg, R. and R. S. Muller, "Space-Change-Limited Currents and Schottky -Emission-Currents in Thin-Film CdS Diodes," Solid-State Electronics, Vol. 7, No. 8, (August 1964), pp. 575-582.